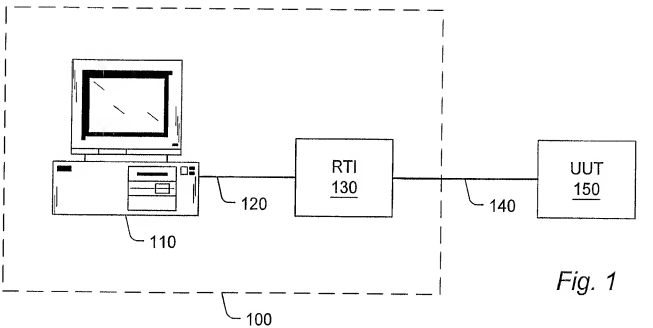


Fig. 1

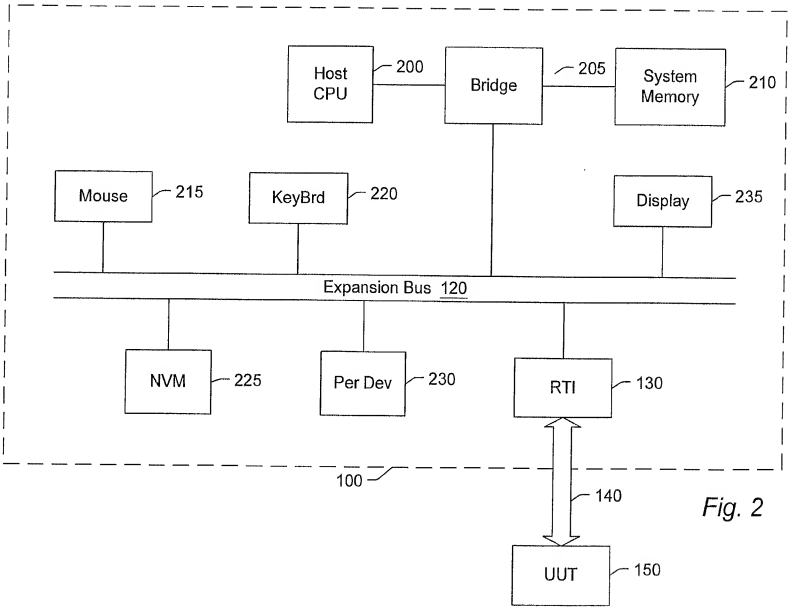

Host CPU
200
Bridge
205
System Memory
210
Mouse
215
KeyBrd
220
Display
235
Expansion Bus 120
NVM
225
Per Dev
230
RTI
130
100
140
UUT
150

Fig. 2

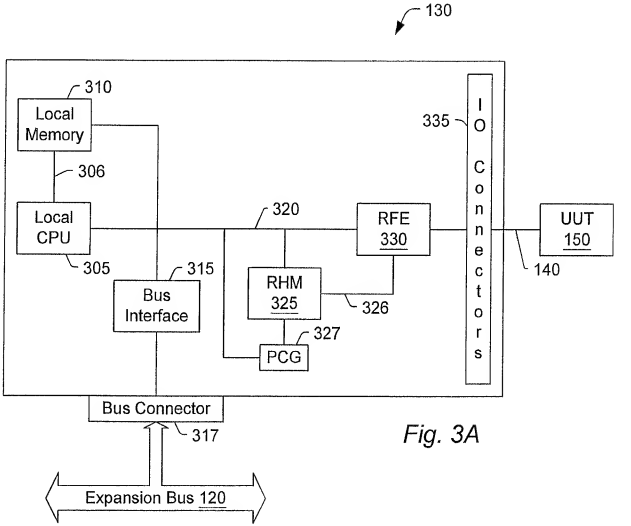

130
310
Local Memory
306
Local CPU
305
315
Bus Interface
320
RHM 325
326
327
PCG
RFE 330
335
I O C o n n e c t o r s
UUT 150
140
Bus Connector
317
Expansion Bus 120

Fig. 3A

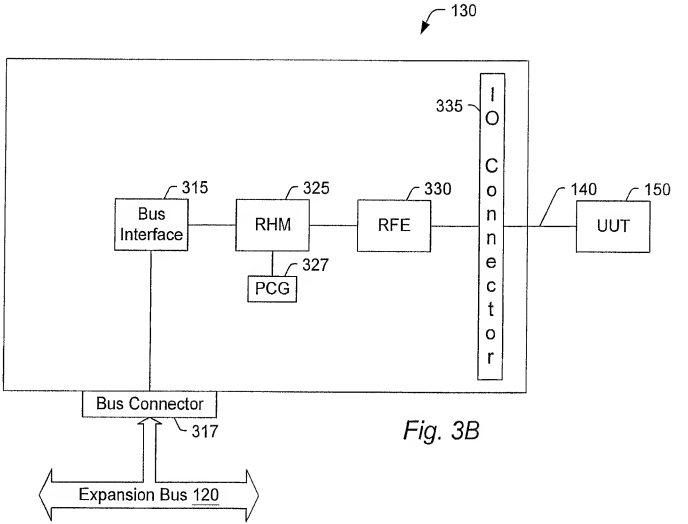


Fig. 3B

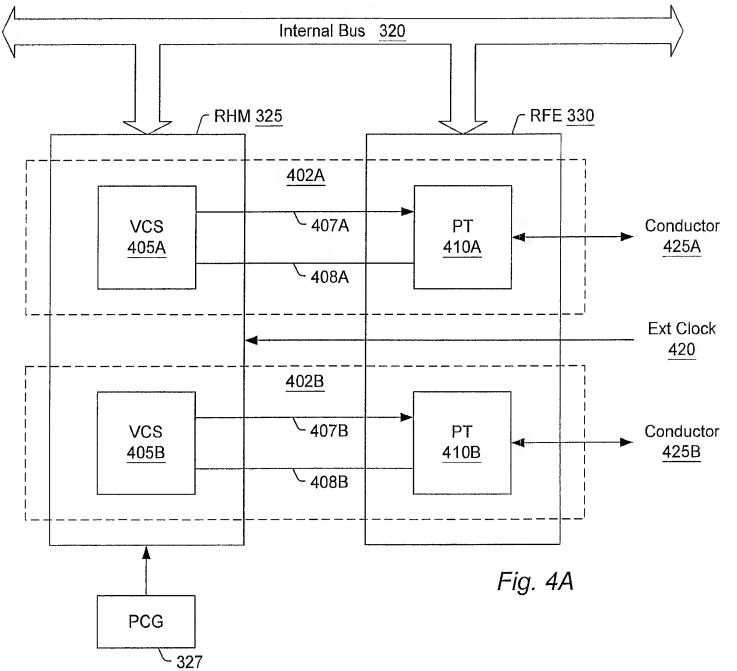

Internal Bus 320
RHM 325
RFE 330
402A
VCS 405A
407A
408A
PT 410A
Conductor 425A
Ext Clock 420
402B
VCS 405B
407B
408B
PT 410B
Conductor 425B
PCG
327

Fig. 4A

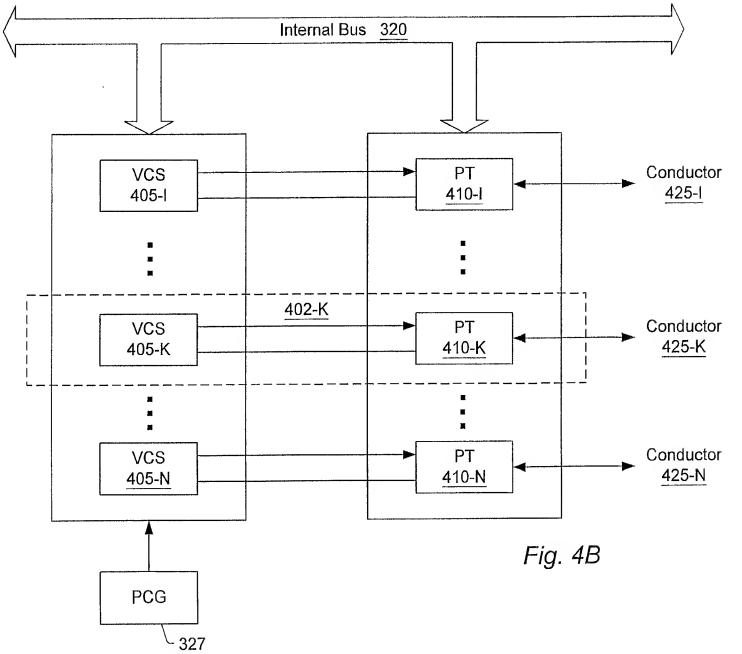
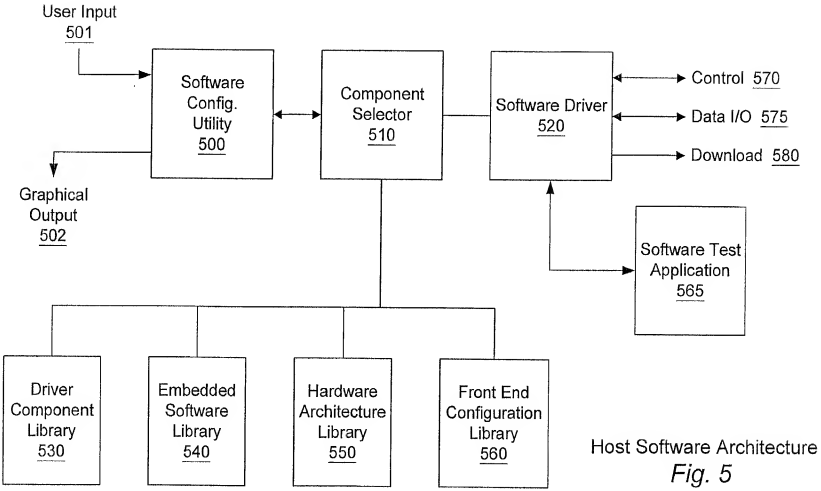

Internal Bus 320
VCS 405-I
PT 410-I
Conductor 425-I
402-K
VCS 405-K
PT 410-K
Conductor 425-K
VCS 405-N
PT 410-N
Conductor 425-N
PCG
327

Fig. 4B



Host Software Architecture

Fig. 5

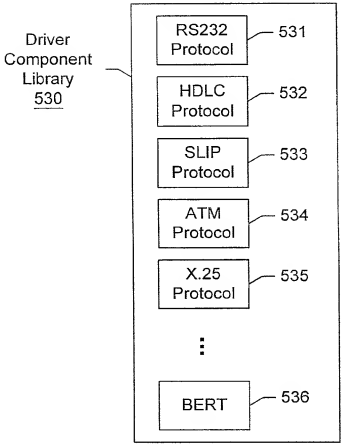


Fig. 6A

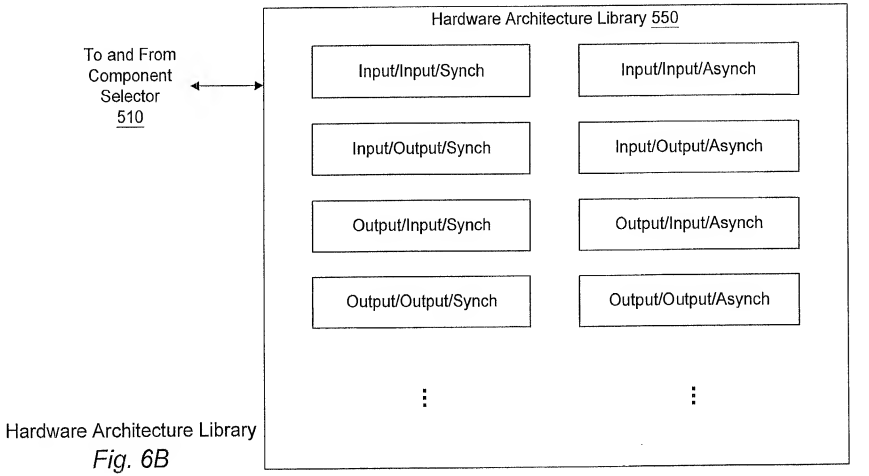

Hardware Architecture Library 550
To and From Component Selector 510
Input/Input/Synch
Input/Input/Asynch
Input/Output/Synch
Input/Output/Asynch
Output/Input/Synch
Output/Input/Asynch
Output/Output/Synch
Output/Output/Asynch
Hardware Architecture Library

Fig. 6B

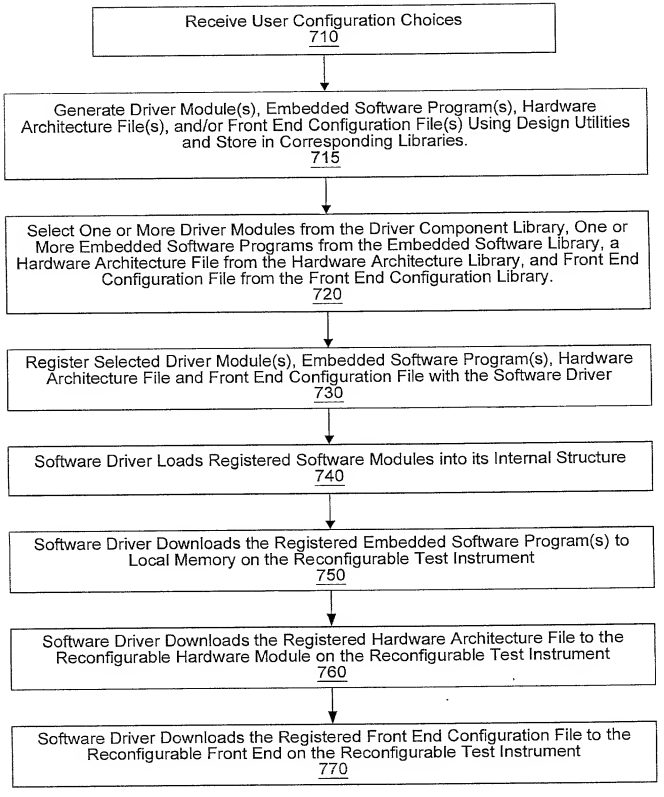
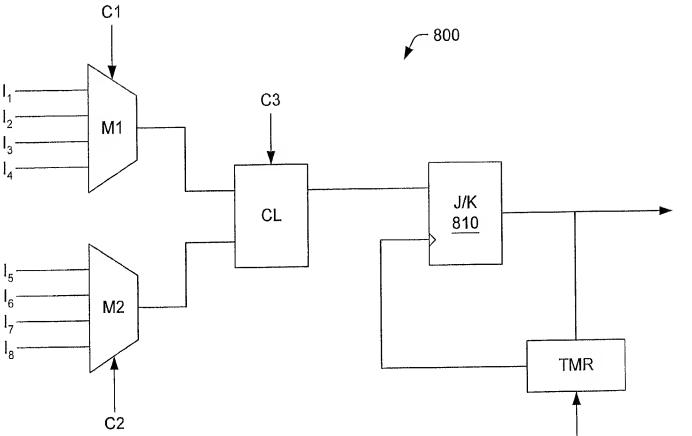


Fig. 7



Programmable Trigger Circuit

Fig. 8